AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A flash memory cell comprising:

a substrate comprising a source and a drain;

a layer comprising a silicon material and adjacent said substrate;

~~a gate element; and~~

a dielectric layer adjacent said silicon dioxide layer ~~between said substrate and said gate element~~, said dielectric layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide;

a floating gate adjacent said dielectric layer;

an oxide-nitride-oxide (ONO) layer adjacent said floating gate; and

a control gate adjacent said ONO layer.

2. (Canceled).

3. (Currently Amended) The flash memory cell of Claim 1 [[2]] wherein said silicon ~~interfacing~~ material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

4-6. (Canceled).

7. (Original) The flash memory cell of Claim 1 wherein said dielectric material comprises a metal oxide.

8. (Original) The flash memory cell of Claim 1 wherein said dielectric layer comprises a composite of a metal oxide and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

9. (Canceled).

10. (Currently Amended) A flash memory array comprising memory cells, wherein a memory cell comprises:

a substrate comprising a source and a drain;

~~a gate element; and~~

a tunnel oxide layer adjacent ~~between~~ said substrate ~~and said gate element~~, said tunnel oxide layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide;

a layer comprising a silicon material and adjacent said tunnel oxide layer;

a floating gate adjacent said dielectric layer;

an oxide-nitride-oxide (ONO) layer adjacent said floating gate; and

a control gate adjacent said ONO layer.

11. (Canceled).

12. (Currently Amended) The flash memory array of Claim 10 [[11]] wherein said silicon ~~first interfacing material and said second interfacing~~ material is ~~are~~ selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

13. (Currently Amended) The flash memory array of Claim 10 wherein said dielectric material comprises a metal oxide.

14-20. (Canceled).

21. (New) A flash memory cell comprising:

a substrate comprising a source and a drain;

a first layer comprising a first silicon material and adjacent said substrate;

a dielectric layer adjacent said silicon dioxide layer, said dielectric layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide;

a second layer comprising a first silicon material and adjacent said dielectric layer;

a floating gate adjacent said second silicon dioxide;

an oxide-nitride-oxide (ONO) layer adjacent said floating gate; and

a control gate adjacent said ONO layer.

22. (New) The flash memory cell of Claim 21 wherein said first silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

23. (New) The flash memory cell of Claim 21 wherein said second silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

24. (New) The flash memory cell of Claim 21 wherein said dielectric material comprises a metal oxide.

25. (New) The flash memory cell of Claim 21 wherein said dielectric layer comprises a composite of a metal oxide and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.